A Hardware-oriented FDTD Algorithm for Sound Field Rendering

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1. Introduction

Sound field rendering is becoming more and more important in some applications. Many algorithms based on computer simulation have been proposed for sound field rendering, such as acoustical ray tracing¹⁾, image source method²⁾, beam tracing method³⁾, finite element method⁴⁾, boundary element method⁵⁾, and finite difference time-domain (FDTD)⁶⁾. Although these algorithms are well defined and accurate for certain applications, their common drawbacks are the intense computations and the high memory requirements as a sound space increases. Due to the limited memory bandwidth of current general-purpose computer systems, such simulations will take a long time. An alternative solution is to implement the sound field rendering algorithms directly by hardware. In our previous work, the Digital Huygens' Model was proposed for the Field Programmable Gate Array (FPGA) based two dimensional sound field rendering^{7,8)}. In this paper, the RMWE-FDTD algorithm is introduced for three dimensional sound field rendering.

In the hardware-based sound field rendering system, a sound space is divided into lots of uniform cubic elements. A uniform computing cell designed based on the rendering algorithm is located in each element to calculate the sound pressure. Typically, a computing cell is required to match the following conditions to improve the system performance.

- (1) The computing cell runs at as fast as possible to reduce the calculation time.
- (2) The computing cell consumes small hardware resources.

Based on these requirements, the sound field rendering algorithm must be as simple as possible, i.e. without complex arithmetic operations involved, such as multiplication and division, since these operations consume more hardware sources, and degrade system clock due to long route delay.

2. RMWE-FDTD Algorithm

In a cubic element, sound wave propagation is

$$\frac{\partial^2 p}{\partial t^2} = c^2 \left(\frac{\partial^2 p}{\partial x^2} + \frac{\partial^2 p}{\partial y^2} + \frac{\partial^2 p}{\partial z^2} \right)$$
(1)

where p denotes the sound pressure, c is the sound speed, x, y, and z are directions of an x-y-z Cartesian coordinate system.

By applying the center differential method in equation (1), and let $\Delta x = \Delta y = \Delta z = \Delta l$, then

$$P^{n+1}(i, j, k) = 2P^{n}(i, j, k) - P^{n-1}(i, j, k) + \chi^{2}[P^{n}(i+1, j, k) + P^{n}(i-1-1-k)] + P^{n}(i-1-1-k) + P^{n}(i-1-1-k)$$
(2)

$$+P^{n}(i, j, k+1) + P^{n}(i, j, k-1) - 6P^{n}(i, j, k)]$$

where $\chi = c\Delta t/\Delta I$ denotes the Courant number. For a three dimensional sound space, $\chi \leq 1/\sqrt{3}$. When χ is $1/\sqrt{3}$, equation (2) is the same as the standard leapfrog Yee-FDTD¹²⁾ and the updated DHM¹⁰⁾.

To eliminate the multiplication operation, χ is assumed to be 1/2, then equation (2) is changed as.

$$P^{n+1}(i,j,k) = \frac{1}{4} [P^n(i+1,j,k) + P^n(i-1,j,k) + P^n(i,j+1,k)]$$
(3)

 $+P^{n}(i, j-1, k)+P^{n}(i, j, k+1)+P^{n}(i, j, k-1)+2P^{n}(i, j, k)]-P^{n-1}(i, j, k)$ In equation (3), the multiplication operations 2^{m} (m= -2, 1) are implemented by shift operations. In contrast with equation (2), equation (3) consists of six additions, one subtraction, and two shift operations.

3. System Performance

3.1 Memory requirement

From equation (3), the sound pressures of elements in the current time step and the previous one time step are stored during calculation. If the number of elements is N, and data width is 32-bit, the memory requirement, the number of operations and memory access in different algorithms are shown in **Table I**. Except the sound pressures of elements in the current time step are kept, the particle velocity at x, y, and z directions are stored in the algorithm Yee-FDTD^{9,13)}, and the scatterings at six directions are required in the original DHM^{10,11)}. This results in more memory and operation requirements for the Yee-FDTD and

governed by the following formula:

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original DHM algorithms¹³⁾. Although the number of operations is the least in the updated DHM, a multiplication operation is included. Compared with other algorithms, the RMWE-FDTD algorithm needs smallest memory, relatively less memory access and operations, and has no multiplication involved.

Table I Memory requirement, operations, and memory access in different algorithms

	Memory	Operations		Memory
Algorithm	(byte)	Total	Multiplication	access
Yee -FDTD	16N	13	0	18
Original DHM	48N	12	1	13
Updated DHM	8N	7	1	8
REWE-FDTD	8N	9	0	9

3.2 Computational results

To verify the validity of the proposed algorithm, a sound space with 32768 ($32 \times 32 \times 32$) elements surrounded by rigid walls is examined and a related sound field rendering system based on the proposed algorithm is developed by both software and hardware. In the sound space, an incident source is located at the point (16, 16, 16), and the observation point is at the point (16, 16, 14). The incident source is a single-shot sine wave with amplitude of 10^8 Pa and 16 samples taken at each period. The calculated time steps are 160. The system is simulated by both software and hardware. The software simulation is developed using the C++ programming language, and the hardware system is synthesized in **FPGA** chip Xilinx а XC5VLX330T-FF1738, and simulated by the EDA tool called Modelsim. In the software simulation, the data are integers while they are 32-bit fixed point in the hardware simulation. Fig. 1 shows the sound pressure at the observation point in both the hardware and software simulations. Except for the one cycle delay, the hardware simulation results agree well with those of the software simulation.



Fig. 1 Wave at the observation point

3.3 Calculation time

In order to evaluate the calculation performance and make a comparison, systems based on different rendering algorithms are developed by C++. In these systems, data are 32-bit floating-point. And the sound space, incident signal, and observation point, are same as the previous ones except the calculation time steps are 20,000. The simulation environment is a computer with an AMD Phenom 9500 Quad-core processor (CPU frequency: 2.2 GHz) and 4Gb RAM. The calculation time taken by different algorithms is presented in **Table II**.

In Table II, the courant number χ is $1/\sqrt{3}$ in the updated DHM and Yee-FDTD, thus their rendering equations are the same, and systems take the same time. The RMWE-FDTD speeds up about 19% (11.95/10.01-1) against the updated DHM and Yee-FDTD, and about 132% (23.23/10.01-1) against the original DHM in computions, respectively. This performance enhancement results from no complicated multiplication operations involved in the RMWE-FDTD.

Table II Execution time taken by different algorithms (s)

Element		Original	Updated	
Scale	RMWE-FDTD	DHM	DHM	Yee-FDTD
$32 \times 32 \times 32$	10.01	23.23	11.95	11.95

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